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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,496	JANZEN, JEFFREY W.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *72-82 and 84-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *72-82 and 84-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on September 15, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Preliminary Amendment

The preliminary amendment of September 15, 2003 cancelled claims 1-71. Claims 72-82 and 84-87 were added. Applicants Remarks of September 15, 2003 recited that claims 72-87 were added. The Examiner would like to point out that a claim 83 was not included in the amendment, and encourages the Applicant to correct the numbering of claims in a future Response.

Claim Objections

Claims 78, 82, and 84-87 are objected to because of the following informalities:

Regarding claim 78, line 2: Replace "aid" with –said-- in order to provide proper antecedent basis.

Regarding claim 82, line 3: Replace "a" with –at an-- in order to clarify the language of the claim.

Regarding claim 84, line 2: Insert –said-- before "input" in order to provide proper antecedent basis.

Regarding claim 85, line 9: Replace "aid temporary" with –said temporary storage-- in order to provide proper antecedent basis.

Regarding claims 86 and 87, line 1: Insert –said-- before "input" in order to provide proper antecedent basis.

Claims 86 and 87 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim (Claim 84). Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Dependent claims 86 and 87 depend upon, and are identical to, parent claim 84.

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 72-76, 81, 82, and 84-87 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 8-13, 15, 17, 21, 26-30, 33, 35, 40, 47-49, and 51-53 of U.S. Patent No. 6,647,470. Although the conflicting claims are not identical, they are not patentably distinct from each other because the current application, as amended according to Applicant's Amendment of September 15, 2003, still reads upon the aforementioned patent.

With respect to claim 72 of the instant application and claim 1 of U.S. Patent No. 6,647,470, the side-by-side analysis is as follows:

U.S. Application No. 10/661,496	U.S. Patent No. 6,647,470
72. A method for writing data to a memory device, comprising:	1. A memory circuit comprising: a data buffer coupled to a storage array of said memory circuit;
issuing a write command to the memory device; issuing input data to the memory device;	a logic circuit for receiving input data associated with a write command, said logic circuit being coupled to said data buffer and said storage array;
issuing a control signal to the memory device;	a command decoder coupled to said logic circuit and said data buffer, said command decoder providing a first control signal to said logic circuit;
wherein when said control signal is in a first state the memory device is caused to perform a write operation while posting said input data (i) and when	wherein when said input data associated with said write command is received by said logic circuit, said logic circuit in response to a first control signal sends said input data directly to said storage array (ii) or sends said input data to said data buffer (i)

said control signal is in a second state the memory device is caused to perform a write operation without posting said input data (ii).	and if said input data is sent to said data buffer, said command decoder sends a second control signal to said data buffer at a predetermine time when input/output gates associated with said storage array are not being used, and said data buffer in response to said third control signal sending said input data from said data buffer to said storage array.

As disclosed above, the disclosure of the instant application and U.S. Patent No. 6,647,470 are identical. Accordingly, there is clearly a commonly disclosed embodiment in the application and the patent.

The following paragraphs list how the claim limitations of the current application map to the claim limitations of the patent. The use of parenthesis, e.g. (1&5), is intended to recite that the combination of claims 1 and 5, where claim 5 is dependent upon claim 1, contain all of the claim limitations of the corresponding application claim, which in this instance is claim 73.

Claim(s) (1), (8), (26), and (47) of patent #6,647,970 contain(s) every element of claim(s) 72 and 81 of the instant application and as such anticipate(s) claim(s) 72 and 81 of the instant application.

Claim(s) (1&5) and (47-49) of patent #6,647,970 contain(s) every element of claim(s) 73 of the instant application and as such anticipate(s) claim(s) 73 of the

instant application.

Claim(s) (1&6), (8-12), (26-30), and (47,48,50) of patent #6,647,970 contain(s) every element of claim(s) 74 of the instant application and as such anticipate(s) claim(s) 74 of the instant application.

Claim(s) (1), (8-13,15,17), (26,27,33,35), and (47,48,50-52) of patent #6,647,970 contain(s) every element of claim(s) 75 of the instant application and as such anticipate(s) claim(s) 75 of the instant application.

Claim(s) (40&41) and (58) of patent #6,647,970 contain(s) every element of claim(s) 76 of the instant application and as such anticipate(s) claim(s) 76 of the instant application.

Claim(s) (1&2), (8-13), (26-31), (47-49,51-53) of patent #6,647,970 contain(s) every element of claim(s) 82 of the instant application and as such anticipate(s) claim(s) 82 of the instant application.

Claim(s) (8-13,15,17), (26,27,33,35), and (47-49,51-53) of patent #6,647,970 contain(s) every element of claim(s) 84, 86, and 87 of the instant application and as such anticipate(s) claim(s) 84, 86, and 87 of the instant application.

Claim(s) (1&2), (8-13), (21), (40), and (47-49,51-53) of patent #6,647,970 contain(s) every element of claim(s) 85 of the instant application and as such anticipate(s) claim(s) 85 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 72-82 and 84-87 are rejected under 35 U.S.C. 102(e) as being anticipated by Shepherd et al. (US# 6,434,665).

Regarding claim 72, Shepherd et al. teaches a **system for writing data to a memory device** (cache subsystem) (col. 4, lines 1-3). **Write commands** (operations) **are issued** (sent) **to the memory device, and input data** (store data) **is issued to the memory device** (col. 4, lines 18-28 & 40-42).

The memory device **performs a write operation while posting said input data** (storing the data in the Store Buffer) **in response to detecting** that a read operation follows the current write operation (which would inherently require **issuing a control signal** to have a value (**in a first state**) indicating which operational path to select should a read operation follow a write operation [Figs. 2 & 4]) (col. 5, lines 13-20 & 60-63; col. 8, lines 1-3 & 36-38). If the next operation is detected to not be a read operation, the inherent **control signal would have a second** value (**state**), and that **within the memory device a write operation occurs** and would store data into memory (228) **without posting the input data** (into store buffer 220) (col. 4, lines 62-65).

Regarding claim 73, Shepherd et al. teaches that the **control signal has a second state if a next command following the write command is another write command** (not a read command), as recited above (col. 4, lines 62-65; Fig. 4).

Regarding claim 74, Shepherd et al. teaches that the **control signal has a first state if a next command following the write command is a read command,** as recited above (col. 5, lines 13-20; Fig. 4).

Regarding claim 75, Shepherd et al. teaches that **the write operation while posting input data includes storing said input data in a temporary storage area** (store buffer 220), and **writing said input data from said temporary storage area to**

an array of said memory device when input/output gates associated with said array are not being used (col. 5, lines 15-20). The input/output gates as claimed refer to the 1) input port on the upper left side of data memory 228 which is coupled to store buffer 220, and 2) the output port of data memory 228 coupled to mux 240 [Figure 2]. Data is sent from the temporary storage area to the memory device when the ports are not being used for another operation because if the ports were presently being used the data would be unable to be accepted at the input port of data memory 228.

Alternatively, the input/output gates as claimed may refer to the a memory's sense amplifiers (not shown for data memory 228) required for the transmission and latching of data into and out of the memory for read and write operations.

Regarding claim 76, Shepherd et al. teaches a **system for writing data to a memory device** (cache subsystem) (col. 4, lines 1-3). Shepherd et al. teaches **determining a next command following a write command** (col. 4, lines 62-65; col. 8, lines 1-3).

If the next command is a read command (operation), The memory device **performs a write** operation **while posting said input data** (storing the data in the Store Buffer [Figs. 2 & 4]) (col. 5, lines 13-20 & 60-63; col. 8, lines 1-3 & 36-38). **If the next command** (operation) **is not a read command** (operation), **the memory device performs a write operation** and store data into memory (228) **without posting the input data** (into store buffer 220) (col. 4, lines 62-65).

Regarding claim 77, Shepherd et al. teaches that a write command followed by a read command requires a special instruction path [Figure 4, steps 408, 412, and 416] not required for normal write operations followed by other write operations. Therefore, **when the memory device performs a write** operation **while posting said input data**, the write-followed-by-read operations **issued to the memory device** would constitute **a posted write command** according to the claim limitations.

Regarding claim 78, Shepherd et al. teaches **causing the memory device to perform a write while posting said input data** includes **write commands** (operations) **issued** (sent) **to the memory device** (col. 4, lines 18-28 & 40-42). The memory device performs a write operation while posting said input data (storing the data in the Store Buffer) in response to detecting that a read operation follows the current write operation, which would inherently require **issuing a control signal** to have a value (**in a first state) within the memory device** (136)) indicating which operational path to select should a read operation follow a write operation [Figs. 2 & 4]) (col. 5, lines 13-20 & 60-63; col. 8, lines 1-3 & 36-38).

Regarding claim 79, Shepherd et al. teaches **causing the memory device to perform a write without posting said input data** includes **write commands** (operations) **are issued** (sent) **to the memory device** (col. 4, lines 18-28 & 40-42).

Regarding claim 80, Shepherd et al. teaches that **causing the memory device to perform a write without posting said input data further includes** that if the memory device detects that the next operation is detected to not be a read operation, **the** inherent **control signal would be issued having a second** value (**state**) **within the memory device**, and that within the memory device a write operation occurs and would store data into memory (228) without posting the input data (into store buffer 220) (col. 4, lines 62-65).

Regarding claim 81, Shepherd et al. teaches a **system for operating a memory device** (cache subsystem) (col. 4, lines 1-3). **Write commands** (operations) **are received at the memory device**, **and input data** (store data) **associated with the write command is received** (col. 4, lines 18-28 & 40-42).

A control signal associated with (related to) **the write command is received which determines whether to process the write command by directly writing said input data to an array** (data memory [228]) (if the next operation is detected to not be a read operation) **of said memory device** (col. 4, lines 62-65), **or by posting said input data to a temporary storage area** (store buffer [220]) (if a read operation is detected to follow the current write operation) **before writing said input data to the array** [Figs. 2 & 4] (col. 5, lines 13-20 & 60-63; col. 8, lines 1-3 & 36-38), **based on a state of said control signal** (which is inherently required in order to determine which operational path to select should a read operation follow a write operation).

Regarding claim 82, Shepherd et al. teaches **that when the input data is posted to the temporary storage area** (store buffer [220]), **an address associated with the input data is written to a second temporary storage area** (store address location 312-1 of store buffer entry 320-1) and **said writing to the array is performed at the address of the array according to said address** (col. 5, lines 15-20 & 61-63; col. 8, lines 1-35).

Regarding claim 84, Shepherd et al. teaches **writing said input data from said temporary storage area to an array of said memory device when input/output gates associated with said array are not being used** (col. 5, lines 15-20). The input/output gates as claimed refer to the 1) input port on the upper left side of data memory 228 which is coupled to store buffer 220, and 2) the output port of data memory 228 coupled to mux 240 [Figure 2]. Data is sent from the temporary storage area to the memory device when the ports are not being used for another operation because if the ports were presently being used the data would be unable to be accepted at the input port of data memory 228. Alternatively, the input/output gates as claimed may refer to the a memory's sense amplifiers (not shown for data memory 228) required for the transmission and latching of data into and out of the memory for read and write operations.

Regarding claim 85, Shepherd et al. teaches a **system for operating a memory device** (cache subsystem) (col. 4, lines 1-3 **Write commands** (operations) **are**

received at the memory device, and input data (store data) **associated with the write command is received** (col. 4, lines 18-28 & 40-42).

A control signal associated with (related to) the write command is received which **determines whether said write command is an ordinary write command or a posted write command if said write command is determined to be an ordinary write command,** the system will **process the write command by directly writing said associated input data to an array** (data memory [228]) (if the next operation is detected to not be a read operation) **of said memory device** (col. 4, lines 62-65). **If said write command is determined to be a posted write command,** the system will **process the write command by writing said associated input data to a temporary storage area** (store buffer [220]) (if a read operation is detected to follow the current write operation) **before writing said associated input data from the temporary storage area to the array of the memory device** [Figs. 2 & 4] (col. 5, lines 13-20 & 60-63; col. 8, lines 1-35).

Regarding claim 86, Shepherd et al. teaches **writing said input data from said temporary storage area to an array of said memory device when input/output gates associated with said array are not being used** (col. 5, lines 15-20). The input/output gates as claimed refer to the 1) input port on the upper left side of data memory 228 which is coupled to store buffer 220, and 2) the output port of data memory 228 coupled to mux 240 [Figure 2]. Data is sent from the temporary storage area to the memory device when the ports are not being used for another operation because if the

ports were presently being used the data would be unable to be accepted at the input port of data memory 228. Alternatively, the input/output gates as claimed may refer to the a memory's sense amplifiers (not shown for data memory 228) required for the transmission and latching of data into and out of the memory for read and write operations.

Regarding claim 87, Shepherd et al. teaches **writing said input data from said temporary storage area to an array of said memory device when input/output gates associated with said array are not being used** (col. 5, lines 15-20). The input/output gates as claimed refer to the 1) input port on the upper left side of data memory 228 which is coupled to store buffer 220, and 2) the output port of data memory 228 coupled to mux 240 [Figure 2]. Data is sent from the temporary storage area to the memory device when the ports are not being used for another operation because if the ports were presently being used the data would be unable to be accepted at the input port of data memory 228. Alternatively, the input/output gates as claimed may refer to the a memory's sense amplifiers (not shown for data memory 228) required for the transmission and latching of data into and out of the memory for read and write operations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related data posting systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

May 27, 2004

Brian R. Peugh
Patent Examiner
Art Unit 2187